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APPLICATION FOR

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FOR

PARALLEL-TUNED ELECRONIC BALLAST

S P E C I F I C A T I O N

TO ALL WHOM IT MAY CONCERN:

Be it known that I, OLE KRISTIAN NILSSEN, a citizen of Norway, residing at Caesar Drive, Route 5, Barrington, Illinois, County of Cook, United States of America, have invented an improved

501 PARALLEL-TUNED ELECTRONIC BALLAST

of which the following is a specification.

BACKGROUND OF THE INVENTION

Field of Invention

The present invention relates to a self-oscillating parallel-tuned transistor inverter ballast, particularly of a kind that comprises bridge-type inverter means.

Description of Prior Art

Although self-oscillating parallel-tuned transistor inverter ballasts do presently exist -- as for instance described in U.S. Patent No. 4,277,726 to Burke -- bridge-type inverters of that type do not presently exist.

SUMMARY OF THE INVENTION

Objects of the Invention

An object of the present invention is that of providing a self-oscillating inverter ballast for powering a gas discharge lamp means.

Another object is that of providing an inverter ballast that is particularly cost-effective, efficient and versatile in use.

These, as well as other important objects and advantages of the present invention will become apparent from the following description.

Brief Description

In its preferred embodiment, subject invention is a full-bridge inverter comprising four switching transistors and being symmetrically powered from a center-tapped DC voltage source through an inductor means having two windings on a single magnetic core -- with one winding positioned in each leg of the DC source. This full-bridge inverter has a center-tapped parallel-resonant L-C circuit connected across its output, and

is made to self-oscillate by way of two positive feedback current-transformers, each connected in series with the center-tapped L-C circuit and a fluorescent lamp load connected thereto.

The outputs from the current-transformers are applied to the control terminals of the four switching transistors, thereby providing load-proportional drive to these transistors.

The center-tapped DC voltage source, the inductor means and the full-bridge inverter circuit with its two feedback current-transformers are connected together in symmetrical fashion; which provides for the center-tap of the inverter output to be at the same potential as the center-tap of the DC voltage source. Thus, since the center-tap of the DC source is grounded, the center-tap of the inverter's output is grounded as well; which, in turn, implies that any load connected to the inverter's output is symmetrically referenced to ground.

The feedback current-transformers are saturable and so designed as to saturate approximately at the time the inverter's output voltage reaches zero magnitude.

A Zener-type voltage-limiting device is connected directly between the inverter's DC power input terminals, thereby to protect the transistors from voltage transients of excessive magnitude.

The fluorescent lamp means is connected with the inverter's output by way of a current-limiting capacitor.

Brief Description of the Drawings

Fig. 1 schematically illustrates the preferred embodiment of the invention.

Fig. 2 shows various voltage waveforms associated with the preferred embodiment of the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Details of Construction

Fig. 1 shows an AC power supply S, which in reality is an ordinary 120Volt/60Hz electric utility power line.

One terminal of power supply S is grounded and also directly connected to a junction J between two energy-storing capacitors C1 and C2. The other terminal of power supply S is connected to the anode of a rectifier R1 and to the cathode of a rectifier R2. Rectifier R1 has its cathode connected to one terminal of C1 -- the other terminal of C1 being connected to junction J. Rectifier R2 has its anode connected to one terminal of C2 -- the other terminal of C2 being connected to junction J.

An inductor means IM has two equal but separate windings W1 and W2: W1 is connected between the cathode of rectifier R1 and a junction B+ between the collectors of two transistors Q1a and Q1b; W2 is connected between the anode of R2 and a junction B- between the emitters of two transistors Q2a and Q2b.

A Zener diode Z is connected between junction B+ and junction B-.

Transistor Q1a is connected with its emitter to a junction Ja, as is also the collector of transistor Q2a. Transistor Q1b is connected with its emitter to a junction Jb, as is also the collector of transistor Q2b.

A center-tapped inductor L is connected between inverter output terminals Oa and Ob. Connected in parallel with L is a capacitor C. The center-tap on inductor L, which is referred-to as inverter reference terminal IRT, is grounded.

Primary winding PW1 of saturable current-transformer SCT1 is connected between junction Jb and output terminal Ob. Primary winding PW2 of saturable current-transformer SCT2 is connected between junction Ja and output terminal Oa.

One secondary winding SW1a of transformer SCT1 is connected between the base and the emitter of transistor Q1a; another secondary winding SW1b of transformer SCT1 is connected between the base and the emitter of transistor Q1b.

One secondary winding SW2a of transformer SCT2 is connected between the base and the emitter of transistor Q2a; another secondary winding SW2b of transformer SCT2 is connected between the base and the emitter of transistor Q2b.

A series-combination of a ballasting capacitor BC and a gas discharge lamp GDL constitutes a load LD; which load is connected across output terminals Oa and Ob.

Details of Operation

The operation of the full-bridge inverter circuit of Fig. 1 may be explained as follows.

Source S provides 120Volt/60Hz voltage to the voltage-doubling and rectifying/filtering circuit consisting of R1, R2, C1 and C2. A substantially constant DC voltage of about 320 Volt magnitude then results at the output of this circuit, with the positive side of this DC voltage being present at the cathode of R1 and the negative side being present at the anode of R2.

This substantially constant-magnitude DC voltage is applied by way of inductor means IM and its two windings W1 and W2, poled as indicated, to the DC power input terminals B+ and B- of the full-bridge inverter circuit comprising transistors Q1a, Q1b, Q2a and Q2b.

This inverter circuit is made to self-oscillate by way of positive current feedback provided by saturable current-transformers SCT1 and SCT2, poled as indicated. Thus, the magnitude of the current provided to any given transistor's base-emitter junction is proportional to the magnitude of the current flowing between output terminals Oa and Ob.

The frequency of inverter oscillation is determined by a combination of the saturation characteristics of the saturable current-transformers and the natural resonance frequency of the parallel L-C circuit (as combined with any tuning effects caused by the load connected thereacross).

The saturation characteristics of the saturable current-transformers are substantially identical to one another and so chosen that, when there is no load connected across output terminals Oa and Ob, the waveform of the output voltage is as indicated in Fig. 2a; which waveform is made up of sinusoidal half-waves of voltage, indicated by HW1 and HW2, interconnected with periods of zero-magnitude voltage, indicated by ZM1 and ZM2. This waveform is achieved by making the time-length of the saturation-time required for the saturable current-transformers to reach saturation longer than the time-length of one of the sinusoidal half-waves of voltage. The degree to which the time-length of the saturation-time is longer than the time-length of one of the sinusoidal half-waves of voltage corresponds to the time-length of the periods of zero-magnitude voltage.

In Fig. 2a, each of the sinusoidal half-waves of voltage represents the natural interaction between L and C as fed from a substantially constant current source.

In combination, the two separate but equal windings W1 and W2 of inductor means IM provide for a total inductance that is large enough so that the current flowing through the two windings and into the inverter remains substantially constant during a complete time-period of one cycle of the inverter's oscillation.

That is, the DC current flowing into the B+ junction and out of the B- junction is substantially constant during the interval between point X and point Y in Fig. 2a. Thus, whenever the L-C parallel circuit is connected between B+ and B- -- which it is during the complete time-length of each of the sinusoidal half-waves of voltage -- it is indeed fed from a substantially constant current source.

When a load impedance having a net component of capacitive reactance (such as does LD) is connected across the inverter's output terminals Oa and Ob, capacitive reactance is in effect added to the L-C parallel circuit; which results in the time-lengthening of the sinusoidal half-waves of voltage -- as indicated by Fig. 2b. The more capacitance added this way, the more time-lengthening results.

On the other hand, when a load impedance having a net component of inductive reactance is connected between Oa and Ob, the result would be a time-shortening of the sinusoidal half-waves of voltage.

By having two different load impedances connected between Oa and Ob, and by having these two load impedances be of conjugate nature, there will be no net effect on the length of the period of the sinusoidal half-waves. For instance, by having another gas discharge lamp like GDL connected in series with an inductor having a reactance of the same absolute magnitude as that of ~~CD~~, and by connecting this series-combination in parallel with load LD, the total net load impedance would be resistive and would cause no net shortening or lengthening of the sinusoidal half-waves of voltage.

By making the time-length of the saturation-time of the saturable current-transformers substantially equal to the time-length of one of the sinusoidal half-waves of voltage, the resulting output voltage will be as illustrated in Fig. 2c; which indicates that the net inversion frequency will now be the same as the natural resonance frequency of the L-C parallel circuit (as combined with whatever load impedance might be connected between Oa and Ob).

By making the time-length of the saturation-time of the saturable current-transformers shorter than the time-length of one of the sinusoidal half-waves of voltage, the resulting output voltage will be as illustrated in Fig. 2d; which indicates that the net inversion frequency will now be higher then the natural resonance frequency of the L-C circuit (as combined with whatever load impedance might be connected between Oa and Ob).

Additional Comments

(a) As long as the time-length of the saturation-time of the saturable current-transformers remains equal to or longer than the time-length of one of the sinusoidal half-waves of voltage, the net inversion frequency will not be affected by the addition or removal of a load impedance, such as LD of Fig. 1, regardless of the magnitude of the net reactive impedance thereby added to or subtracted from the L-C parallel circuit.

(b) The magnitude of the Zener voltage of Zener diode Z is chosen such as to be somewhat higher than the maximum magnitude of the peak voltage of the sinusoidal half-waves of voltage present across the inverter's output terminals Oa and Ob. That way, the Zener diode will not interfere with normal operation of the inverter; yet, it will prevent the magnitude of the peak voltages of the sinusoidal half-waves from substantially exceeding the normally occurring maximum magnitudes. Without the Zener diode, for various transient reasons (such as due to the sudden removal of a load) the magnitude of the peak voltages of the sinusoidal half-waves would occasionally become substantially larger than the normally occurring maximum magnitudes; and that would either cause transistor destruction, or it would necessitate the use of very special transistors of exceptionally high voltage capabilities.

(c) Inductor L is center-tapped; which, in effect, provides for a center-tap between the inverter's output terminals Oa and Ob. This center-tap is grounded. In many applications, particularly in the case of fluorescent lamp ballasts, it is very valuable to have the output referenced to ground.

(d) Inductor L may be integrally combined with a center-tapped auto-transformer; in which case the output voltage can readily be provided at any desired magnitude, while maintaining a ground-connected center-tap.

(e) Inductor means IM may consist of two entirely independent inductors -- with one inductor located in each leg of the power supply. In fact, it is even acceptable under some circumstances to use but a single inductor in just one leg of the power supply; in which case, however, it would not be possible to connect the output's center-tap with the power supply's center-tap.

(f) It is not necessary to power the inverter of Fig. 1 from a voltage doubler. However, doing so provides for the advantage in many situations of being able to reference the center-tap of the inverter's output with one of the legs of the power line.

(g) The inverter of Fig. 1 must be triggered into oscillation. This triggering may be accomplished by way of providing a special trigger winding on each of the feedback current-transformers, and then to discharge a capacitor through these trigger windings. This may be done automatically with an arrangement consisting of a capacitor-resistor combination connected between B+ and B-, and a Diac for discharging the capacitor through the trigger windings.

(h) Finally, it is noted that the average absolute magnitude of the AC voltage appearing between inverter output terminals Oa and Ob must be substantially equal to the magnitude of the DC voltage provided from across the two series-connected energy-storing capacitors C1 and C2.

Or, stated differently, in the circuit of Fig. 1, if the inverter's AC output voltage as provided between terminals Oa and Ob were to be rectified in a full-wave rectifier, the average magnitude of the DC voltage obtained from this full-wave rectifier would have to be substantially equal to the magnitude of the DC voltage supplied from the DC output of the rectifier/filter combination consisting of R1, R2, C1 and C2.

This relationship would have to exist substantially regardless of the nature of the load connected between the inverter's output terminals.

(i) Although the full-bridge inverter circuit of Fig. 1 may be designed to invert at any one of a wide range of frequencies, in the preferred embodiment the inversion frequency is approximately 30 kHz. Thus, the time-length of the interval between point X and point Y of Fig. 2a is about 33 micro-seconds.

(j) The waveforms of Fig. 2 depict the voltage present between output terminals Oa and Ob under different operating conditions. Of course, the voltage present between Oa and inverter reference terminal IRT is equal to half the voltage present between terminals Oa and Ob.

(k) Due to the balanced nature of the inverter and its DC power supply, with reference to any one of the terminals of filter capacitors C1 and C2, any high frequency voltage present at inverter reference terminal IRT -- even if it were not connected with ground -- would have negligible magnitude.

(l) The primary windings of saturable current transformers SCT1 and SCT2 have fewer turns than do the secondary windings. Typically, the transistors operate with a 1:4 primary-to-secondary turns ratio; which corresponds to a forced current gain of four. At that turns ratio, the magnitude of the voltage developing across the primary winding of each of the saturable current transformers is only one fourth of the magnitude of the base-emitter voltage; which, of course, is only about 0.8 Volt.

In other words, the magnitude of the voltage developing across the primary winding of each staturable transformer is only about 0.2 Volt; which, of course, represents a magnitude that is totally negligible in comparisn with the magnitude of the voltage developing between output terminals Oa and Ob.

Thus, the voltage at terminal Ob is substantially equal to the voltage at terminal Jb; and the voltage at terminal Oa is substantially equal to the voltage at terminal Ja.

(m) It is believed that the present invention and its several attendant advantages and features will be understood from the preceeding description. However, without departing from the spirit of the invention, changes may be made in its form and in the construction and interrelationships of its component parts, the form herein presented merely representing the presently preferred embodiment.

I claim